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<u>L14</u>	l2 and l5	48	<u>L14</u>
<u>L13</u>	l2 and l4	52	<u>L13</u>
<u>L12</u>	l6 and @py<=1991	1	<u>L12</u>
<u>L11</u>	l2 and @py<=1991	4	<u>L11</u>
<u>L10</u>	l3 and l5	3	<u>L10</u>
<u>L9</u>	L3 and l4	3	<u>L9</u>
<u>L8</u>	l5 and L6	20	<u>L8</u>
<u>L7</u>	l4 and L6	22	<u>L7</u>
<u>L6</u>	(dsp or digital near1 signal) near8 (one or single ) near4 (instruction\$1 or command\$1) near25 general near3 purpose	31	<u>L6</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L5</u>	(712/35-36)![CCLS]	394	<u>L5</u>

<u>L4</u>	(712/30-39 )![CCLS]	1380	<u>L4</u>
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	(dsp or digital near1 signal) near8 (one or single ) near4 (instruction\$1 or		
<u>L3</u>	command\$1) near25 general near3 purpose near3 (process\$3 or	7	<u>L3</u>
	microprocess\$3)		
<u>L2</u>	(dsp or digital near1 signal) near8 (one or single ) near4 (instruction\$1 or	243	<u>L2</u>
	command\$1) and general near3 purpose near3 (process\$3 or microprocess\$3)		
<u>L1</u>	(dsp or digital near1 signal) near8 (one or single ) near4 (instruction\$1 or	1067	<u>L1</u>
	command\$1)		

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(dsp or digital signal) and general purpose and single

☐ Check to search within this result set
**Results Key:****JNL** = Journal or Magazine **CNF** = Conference **STD** = Standard**1 A low-cost media-processor based real-time MPEG-4 video decoder***Jin-Hau Kuo; Chia-Chiang Ho; Kan-Li Huang; Jim Shiu; Ja-Ling Wu;*Consumer Electronics, IEEE Transactions on , Volume: 49 , Issue: 4 , Nov. 2000  
Pages:1488 - 1497
[\[Abstract\]](#) [\[PDF Full-Text \(556 KB\)\]](#) **IEEE JNL**
**2 Real-time software based MPEG-4 video encoder***Weiguo Zheng; Ahmad, I.; Liou, M.L.;*MPEG-4. 2001 Proceedings of Workshop and Exhibition on , 18-20 June 2001  
Pages:71 - 74
[\[Abstract\]](#) [\[PDF Full-Text \(405 KB\)\]](#) **IEEE CNF**
**3 Some fast speech processing algorithms using AltiVec technology***Joshi, S.M.; Dubey, P.K.;*Acoustics, Speech, and Signal Processing, 1999. ICASSP '99. Proceedings., 1999 IEEE International Conference on , Volume: 4 , 15-19 March 1999  
Pages:2135 - 2138 vol.4
[\[Abstract\]](#) [\[PDF Full-Text \(312 KB\)\]](#) **IEEE CNF**
**4 A 51.2-GOPS scalable video recognition processor for intelligent control based on a linear array of 128 four-way VLIW processing elements***Kyo, S.; Koga, T.; Okazaki, S.; Kuroda, I.;*Solid-State Circuits, IEEE Journal of , Volume: 38 , Issue: 11 , Nov. 2003  
Pages:1992 - 2000
[\[Abstract\]](#) [\[PDF Full-Text \(832 KB\)\]](#) **IEEE JNL**

**5 Subword extensions for video processing on mobile systems***Jennings, M.D.; Coate, T.M.;*

Concurrency, IEEE [see also IEEE Parallel &amp; Distributed Technology] , Volume 6 , Issue: 3 , July-Sept. 1998

Pages:13 - 16

[\[Abstract\]](#) [\[PDF Full-Text \(140 KB\)\]](#) IEEE JNL**6 A programmable digital filter IC employing multiple processors on a single chip***Kwentus, A.Y.; Werter, M.J.; Willson, A.N., Jr.;*

Circuits and Systems for Video Technology, IEEE Transactions on , Volume: 2 , Issue: 2 , June 1992

Pages:231 - 244

[\[Abstract\]](#) [\[PDF Full-Text \(1056 KB\)\]](#) IEEE JNL**7 Short vector code generation and adaptation for DSP algorithms***Franchetti, F.; Puschel, M.;*

Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '03). ; IEEE International Conference on , Volume: 2 , 6-10 April 2003

Pages:II - 537-40 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(366 KB\)\]](#) IEEE CNF**8 SVP: scan-line video processor-general purpose video processor***Onuma, H.; Yaguchi, Y.; Miyaguchi, H.; Akiyama, T.; Kajiyama, K.; Adachi, K Kikuchi, A.; Kojima, T.; Narumi, T.;*

VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical Papers., 1995 International Symposium on , 31 May-2 June 1995

Pages:196 - 200

[\[Abstract\]](#) [\[PDF Full-Text \(268 KB\)\]](#) IEEE CNF**9 Efficient FFT implementation on an IEEE floating-point digital signal processor***Kloker, K.L.; Lindsley, B.; Baron, N.; Sohie, G.R.L.;*

Acoustics, Speech, and Signal Processing, 1989. ICASSP-89., 1989 International Conference on , 23-26 May 1989

Pages:1302 - 1305 vol.2

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Mar 5, 2002

US-PAT-NO: 6353863

DOCUMENT-IDENTIFIER: US 6353863 B1

TITLE: Terminal

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 2. Document ID: US 6260088 B1

L10: Entry 2 of 16

File: USPT

Jul 10, 2001

US-PAT-NO: 6260088

DOCUMENT-IDENTIFIER: US 6260088 B1

**\*\* See image for Certificate of Correction \*\***TITLE: Single integrated circuit embodying a risc processor and a digital signal processor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 3. Document ID: US 5872960 A

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File: USPT

Feb 16, 1999

US-PAT-NO: 5872960

DOCUMENT-IDENTIFIER: US 5872960 A

TITLE: Integrated circuit having CPU core operable for switching between two independent asynchronous clock sources of different frequencies while the CPU continues executing instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
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☐ 4. Document ID: US 5685005 A

L10: Entry 4 of 16

File: USPT

Nov 4, 1997

US-PAT-NO: 5685005

DOCUMENT-IDENTIFIER: US 5685005 A

TITLE: Digital signal processor configured for multiprocessing

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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K/MC

☐ 5. Document ID: US 5649208 A

L10: Entry 5 of 16

File: USPT

Jul 15, 1997

US-PAT-NO: 5649208

DOCUMENT-IDENTIFIER: US 5649208 A

TITLE: Mechanism for handling non-maskable interrupt requests received from different sources

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 6. Document ID: US 5630153 A

L10: Entry 6 of 16

File: USPT

May 13, 1997

US-PAT-NO: 5630153

DOCUMENT-IDENTIFIER: US 5630153 A

TITLE: Integrated digital signal processor/general purpose CPU with shared internal memory

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 7. Document ID: US 5613149 A

L10: Entry 7 of 16

File: USPT

Mar 18, 1997

US-PAT-NO: 5613149

DOCUMENT-IDENTIFIER: US 5613149 A

TITLE: Integrated data processing system utilizing successive approximation analog to digital conversion and PWM for parallel disconnect

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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☐ 8. Document ID: US 5611075 A

L10: Entry 8 of 16

File: USPT

Mar 11, 1997

US-PAT-NO: 5611075

DOCUMENT-IDENTIFIER: US 5611075 A

TITLE: Bus architecture for digital signal processor allowing time multiplexed access to memory banks

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 9. Document ID: US 5606714 A

L10: Entry 9 of 16

File: USPT

Feb 25, 1997

US-PAT-NO: 5606714

DOCUMENT-IDENTIFIER: US 5606714 A

TITLE: Integrated data processing system including CPU core and parallel, independently operating DSP module and having multiple operating modes

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 10. Document ID: US 5603017 A

L10: Entry 10 of 16

File: USPT

Feb 11, 1997

US-PAT-NO: 5603017

DOCUMENT-IDENTIFIER: US 5603017 A

TITLE: Parallel integrated circuit having DSP module and CPU core operable for switching between two independent asynchronous clock sources while the system continues executing instructions

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 11. Document ID: US 5592677 A

L10: Entry 11 of 16

File: USPT

Jan 7, 1997

US-PAT-NO: 5592677

DOCUMENT-IDENTIFIER: US 5592677 A

**\*\* See image for Certificate of Correction \*\***TITLE: Integrated data processing system including CPU core and parallel, independently operating DSP module

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KMC
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☐ 12. Document ID: US 5590357 A

L10: Entry 12 of 16

File: USPT

Dec 31, 1996

DOCUMENT-IDENTIFIER: US 5590357 A

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KWMC

May 21, 1996

DOCUMENT-IDENTIFIER: US 5519879 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KVMC

Apr 23, 1996

DOCUMENT-IDENTIFIER: US 5511219 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KMC

Feb 13, 1996

DOCUMENT-IDENTIFIER: US 5491828 A

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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KIMC



☐ 16. Document ID: US 5487173 A

L10: Entry 16 of 16

File: USPT

Jan 23, 1996

US-PAT-NO: 5487173

DOCUMENT-IDENTIFIER: US 5487173 A

TITLE: DTMF detection in an integrated data processing system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments
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